AMENDMENTS TO CLAIMS

- Please delete claims 1-33, 38, 40-46, 52-60, and 62-66.
- Please amend pending claim 61 as indicated below. A complete listing of all claims and their status in the application is as follows:

Claims 1-33 (canceled)

34. (original) A method for forming an ESD protection circuit formed at an input/output interface of an integrated circuit formed on a substrate to protect said integrated circuit from damage caused by an ESD event, said ESD protection circuit comprising:

forming a polycrystalline silicon bounded SCR on a surface of said substrate by the steps of:

forming a first well region lightly doped with impurities of a first conductivity type on a surface of said substrate,

forming a second well region within said first well region by lightly doping said second well region with impurities of a second conductivity type, said impurities of the second conductivity type having a polarity opposite from the impurities of the first conductivity type,

forming a first diffusion region within said second well by heavily doping said first diffusion region with the impurities of the first conductivity type,

forming a second diffusion region within said first well region at a second distance from the first diffusion region by heavily doping said second diffusion region with impurities of the second conductivity type, and

forming a heavily doped polycrystalline layer at the surface of said substrate and between the first and second diffusion regions and astride a junction of the first well region and the second well region to form a bounding component to prevent silicide formation at junctions of the first diffusion region and the second well region, the first well region and the second region, and the second diffusion region and the first well region during fabrication of said silicon controlled rectifier;

connecting said polycrystalline silicon bounded SCR between a signal input/output interface of said integrated circuit and a power supply connection of said integrated circuit;

forming a biasing circuit; and

connecting said biasing circuit to said polycrystalline silicon bounded SCR to bias said polycrystalline silicon bounded SCR to turn on more rapidly during said ESD event.

35. (original) The method of claim 34 further comprising the steps of:

forming at least one diode on said substrate; and

connecting said diode between said signal input/output interface and an anode connection of said polycrystalline silicon bounded SCR to increase a holding voltage for said polycrystalline silicon bounded SCR when said polycrystalline silicon bounded SCR is turned on.

36. (original) The method of claim 34 wherein forming said biasing circuit: comprises the steps of:

forming a polycrystalline silicon bounded diode said polycrystalline silicon bounded diode by the steps of:

forming the first diffusion region,

forming the second well region, and

forming a second heavily doped polycrystalline layer at the surface of said substrate and placed adjacent to the first diffusion region and astride a junction of the second well region and first diffusion region to form a bounding component to prevent silicide formation at said junction of the first diffusion region and the second well region during fabrication of said polycrystalline silicon bounded diode;

wherein said junction of the first diffusion region and the second well region forms said polycrystalline bounded diode; and

connecting said polycrystalline silicon bounded diode to the signal input/output interface,

forming a third diffusion region within said second well by heavily doping said third diffusion region with the impurities of the second conductivity type,

forming a first resistance of material of the second well from a first gate of said polycrystalline silicon bounded SCR to said third diffusion region, and

connecting said third diffusion region to said power supply connection to provide a low resistance path to said second well from said power supply connection.

37. (original) The method of claim 36 wherein forming said biasing circuit further comprises the steps of:

forming a second resistance of the material of the second well from said first gate to said first diffusion region.

38. (canceled)

39. (original) The method of claim 34 wherein said biasing circuit: comprises the steps of:

forming a plurality of serially connected diodes;

connecting a first diode of said plurality of serially connected diodes to the signal input/output interface;

connecting a last diode of said plurality of serially connected diodes to a second gate of said polycrystalline silicon bounded SCR; and

forming a second resistor from the second gate and the last diode of the plurality of serially connected diodes to the power supply connection;

wherein an ESD event causes a current to flow through said plurality of serially connected diodes and said second resistor to trigger the polycrystalline silicon bounded SCR to turn on.

Claims 40-46 (canceled)

47. (original) The method of claim 34 wherein said heavily doped polycrystalline layer of the polycrystalline silicon bounded SCR permits a series resistance of said polycrystalline silicon bounded SCR to be smaller for a more efficient operation.

48. (original) The method of claim 34 further comprising the step of connecting the heavily doped polycrystalline layer to bias said heavily doped polycrystalline silicon layer such that silicide shorting is prevented said first and second diffusion regions and preventing of accidental formation of an inversion region under said heavily doped polycrystalline layer.

49. (original) The method of claim 48 further comprising the step of connecting said heavily doped polycrystalline silicon layer to the second diffusion region.

50. (original) The method of claim 48 further comprising the step of linking the first diffusion region to a voltage source which provides a relatively large voltage during said ESD event which when said relatively large voltage exceeds said snapback voltage, said polycrystalline silicon bounded SCR conducts.

51. (original) The method of claim 49 further comprising the step of linking the first well region, the second well region, said highly doped polycrystalline silicon layer, and the second diffusion to a return of the voltage source.

Claims 52-60 (canceled)

61. (currently amended) ~~The method of claim 60 further comprising the steps of:~~ A method for forming an ESD protection circuit formed at an input/output interface of an integrated circuit formed on a substrate to protect said integrated circuit from damage caused by an ESD event, said ESD protection circuit comprising:

forming a shallow trench isolation bounded SCR on a surface of said substrate;

connecting said shallow trench isolation bounded SCR between a signal input/output interface of said integrated circuit and a power supply connection of said integrated circuit;

forming a biasing circuit;

connecting said biasing circuit to said shallow trench isolation bounded SCR to bias said shallow trench isolation bounded SCR to turn on more rapidly during said ESD event;

forming at least one diode on said substrate; and

connecting said diode between said signal input/output interface and an anode connection of said shallow trench isolation bounded SCR to increase a holding voltage for said shallow trench isolation bounded SCR when said shallow trench isolation bounded SCR is turned on.

Claims 62-66 (canceled)